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Probability Measurement of Setup And Hold Time With Statistical Static Timing Analysis

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ABSTRACT
Statistical static timing analysis (SSTA) plays a key role in determining performance of the VLSI circuits implemented in state-of-the-art CMOS technology. A pre-requisite for employing SSTA is the characterization of the setup and hold times of the latches and flip-flops in the cell library. This paper presents a methodology to exploit the statistical codependence of the setupand hold times. The approach comprises of three steps. In the first step, probability mass function (pmf) of codependent setup and hold time (CSHT) contours are approximated with piecewise linear curves by considering the probability density functions of sources of variability. In the second step, Pmf of the required setup and hold times for each flip-flop in the design are computed. Finally, these Pmf values are used to compute the probability of individual flip-flops in the design passing the timing constraints and to report the overall pass probability of the flip-flops in the design as a histogram. We applied the proposed method to true single phase clocking flip-flops to generate the piecewise linear curves for CSHT. The characterized flip-flops were instantiated in an example design, on which timing verification was successfully performed.

I. I INTRODUCTION

As we move towards the 45nm and lower minimum feature sizes for the devices, process variations are becoming an ever increasing concern for the design of high performance integrated circuits [1]. Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, or republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee. The process variations can cause excessive uncertainty in timingcalculation, which in turn calls for sophisticated analysis techniques to reduce the uncertainty. As the number of sources ofvariations increases, corner-based static timing analysis (STA) techniques computationally become very expensive. Moreover,with decreasing size of transistors and interconnect width, the variation of electrical characteristics is getting proportionallyhigher. The process corner approach, which used to work well, may thus result in inaccurate estimates and over-constrained designs. Statistical static timing analysis (SSTA) has been developed to address the above-mentioned shortcomings of the STA [2] [3]. Operating frequencies of up to 1 GHz are common in modern integrated circuits. As the clock period decreases, inaccuracy in setup/hold times caused by corner-based STA tools becomes less acceptable. Optimism in setup/hold time calculation can result in

circuit failure, while pessimism leads to inferior performance [4].1 Therefore, accurate characterization of the setup and hold times of latches and registers is critically important for timing analysis of digital circuits [5]. Typically in today's circuit design, setup and hold times are characterized independently since these quantities are assumed independent. However, setup and hold times are not independent [4]. In the other words, there are multiple pairs of setup and hold times that result in the same clock-to-q delay. Salman et al. in [4] presented a methodology to co-dependently characterize the setupand hold times of sequential circuit elements and use the resulting multiple pairs in STA. An Euler-Newton curve tracing procedure was used in [5] to efficiently characterize the setup and hold times co-dependently. The set of all codependent setup/hold time pairs which yield the same clock-to-q delay define a contour of the clock-to-q surface. The setup/hold time contours are utilized to evaluate the setup and hold slack2. In a conventional static timing analysis, the STA tool reports the percentage of flip-flops which fail the timing constraints in a circuit based on the number of flipflops which have negative slack. This information is then used by the circuit designer to determine the clock frequency of circuit. With statistical parameter variations becoming more visible in VLSI circuits, delay of every combinational path in the circuit as well as the setup

and hold times of flip-flops (which serve as the start and end points of the combinational paths) become nondeterministic parameters, therefore, values of setup and hold slacks themselves become random variables. The existing statistical STA (SSTA) algorithms consider only the impact of process variation only on the delay of combinational paths in the circuit to estimate the slack of circuit [6]-[7]. However, to perform accurate timing verification and to precisely determine timing violations, theimpact of process variations on the clock-to-output delay and codependent setup/hold times must be considered. This paper presents a statistical CSHT characterization approach by taking into account the impact of process variations. It proposes to efficiently approximate a setup/hold time contour by using a three-point piecewise linear curve. Moreover, this paper proposes a backward Euler based search (BEBS) method to obtain setup/hold times contours. A probability mass function (pmf) is derived for positions of the contours in the setup/hold time plane. Another probability mass function (pmf) is obtained for therandom variable defined on the required setup time (RST) and the required hold time (RHT) of the flip-flop in the circuit. These two pmf's are utilized to obtain the probability that the slack of a flipflop is negative and hence violates the timing constraints. The proposed algorithm enables SSTA to report a set of probability values which accurately represent the percentage of time that the flip-flop fails. In contrast, a STA tool reports a deterministic percentage of flip-flops which fail the setup and hold timeconstraints, and this value may be optimistic or pessimistic for a circuit whose process and circuit parameters are subject to random change. In this article, a methodology to study process variations inducing setup and hold time violations is presented. It is a mix between statistical static timinganalysis (SSTA) [4,5] and Monte Carlo (MC) analysis. Application on a real case, a MAC Multiplier Accumulator, found in many embedded systems requiring high speed calculation, has been made and results given. Process variations on transistor characteristics are the focus of this work. Interconnect variations which are another important topic are notconsidered here.

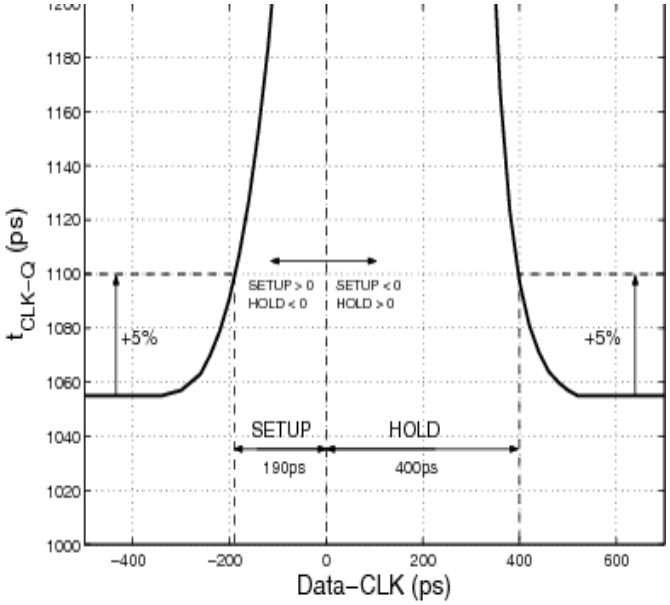

Figure 1. Definitions of setup and hold times.

II. STATIC CSHT

This section provide some terminology, propose a backward Euler based search for characterizing codependent setup hold time contour for a given clock-to-q delay, and explains how to utilize this contour in a STA tool for timing verification.

2.1 Terminology

Latches and flip-flops are the sequential circuit elements used in synchronous designs. The **setup time** is the *minimum time before* the active edge of the clock that the input data line must be valid for reliable latching. Similarly, the **hold time** represents the *minimum time* that the data input must be held stable *after* the active clock edge. The active clock edge is the transition edge (either low-to-high or high-to-low) at which data transfer/latching occurs. The **clock-to-q** delay is the delay from the 50% transition of the active clock edge to the 50% transition of the output, *q*, of the latch/register. The **setup skew** refers to the delay from the latest 50% transition edge of the data signal to the 50% active clock transition edge; similarly, the **hold skew** denotes the delay from the 50% active clock transition edge to the earliest 50% transition edge of the data signal. Figure 1 illustrates the setup and hold skews, which are denoted by $\tau sw$and τhw, respectively. A common technique for setup/hold time characterization is to plot the clock-to-q delay, *tc2q*, for various setup and hold skews via a series of transient simulations. This process in turn produces a clock-to-q *delay surface*. The setup (hold) time is then taken as a particular setup (hold) skew point on the plot, for which the *characteristic clock-to-q delay*1, *tcc2q*, increases by say 10%. As already mentioned, the setup and hold times are not

independent quantities, but depend strongly on one another. Typically, the hold time reduces as the setup skew moves up. Similarly, the setup time decreases as the hold skew increases. The tradeoff between setup and hold skews and the hold and setup times is a strong function.

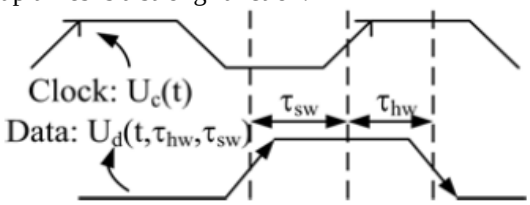

Figure 1. An illustration of the setup and hold skews.

2.2 CSHT Characterization

A general method to extract codependent pairs of setup/hold times is to first obtain the clock-to-q delay, *tc2q*, as a function of the setup/hold skews. This is followed by extraction of a contour of the setup/hold times corresponding to all points on the *tc2q* surface that result in a given increase (*e.g.*, 10%) in the characteristic clock-to-q delay, *tcc2q* [5]. Figure 2 depicts an example setup/hold time contour.

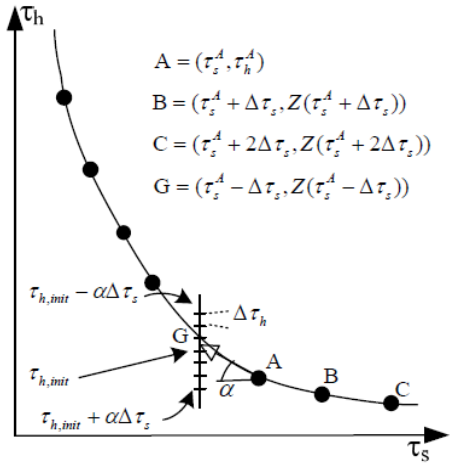

Figure 2. A codependent setup and hold time contour

III. VIOLATION PROBABILITIES ON A CRITICAL PATH

To get an exhaustive comparison of these FF in a functional environment, we were considered a real case. Data and clock paths were extracted from a multiplier design at its place and route level, and then we replaced the initial FF by those of this study. To get the efficiency of one FF, we compute the hold/setup time violation probabilities thanks to the methodology described in [9]. This method allows us to take into account Clk-to-Q delay variations in the same time than setup/hold time variations, and then use all data available in part III. It is based on a SSTA (Statistical Static Timing Analysis) [4-9] for the combinatory paths, mixed with MC timing data coming from the sequential cells. Fig. 2 illustrates the method. We took the longest and the shortest timing path of our design to compute the setup (hold) time violations. We recall that probabilities can be found thanks to the equations given
below :

$$Pv\_setup = \Pr(P - dpath + dclock < dsetup)$$
$$Pv\_hold = \Pr(dpath - dclock < dhold)$$

with*P* the period, *dpath*the delay distribution function of thedata path, *dclock* the delay distribution function of the clock,*dsetup/dhold*the distribution function of the setup/hold time.The worst design case was taken at 1,1V, 125C for the longpath (setup) and the best design case at 1,3V, -40 C for theshort path (hold). Regarding the setup and hold time variationdefinitions, the same design corners were taken for all thesimulations, even if it is hard to predict common worst casesfor all the FFs [9]. However, these differences remain small and the comparison can be relevant.

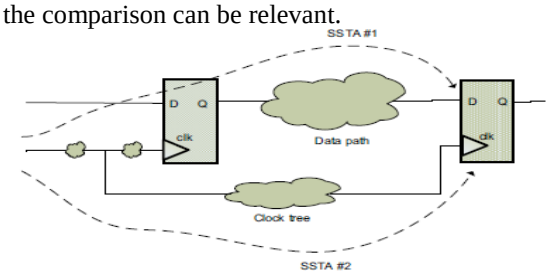

Fig. 3 presents for each FF of this study the setup time

violation probabilities of a critical path. These results showfew differences between the variations of each case,suggesting that intrinsic setup time FF deviations do not play amajor role once integrated into the whole path analysis. On theother hand, the setup time and Clk-to-Q means are majorparameters. The period difference between the worst and thebest flip-flop is about 0,2 ns, equivalent to a performancedifference of about 7%, which can be determining for highspeed chips.

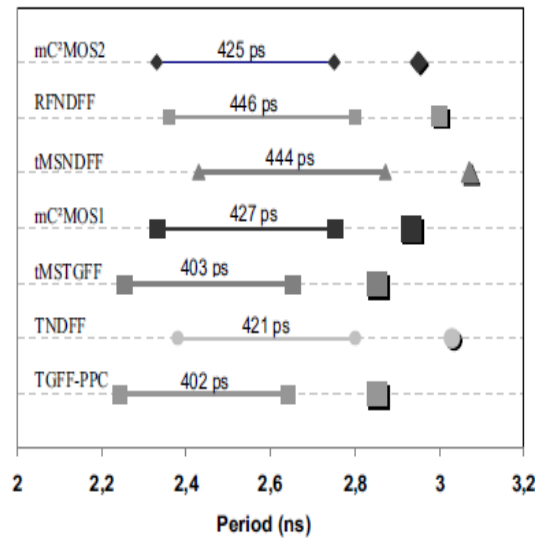

Fig. 3 : This graph represents the period range

corresponding to a setup timeviolation probability between 90% and 10%. The single points refer to aviolation probability of 0.5%.*TGFF-PPC* and *tMSTGFF*are the best flip-flops in this case,beneficiating of the fast Clk-to-Q delay in the data path,combined with a low setup time with weak variations.For the hold time violation probabilities, the only flip-flopswith no negligible probabilities are the *tMSTGFF*(0,29%) andthe *TGFF-PPC* (0,26%). These two FFs have similar Clk-to-Qpaths and data paths, made of transmission gates and inverters.Indeed, hold time depends on clock race until the beginning ofthe second memory point versus data race until this samepoint. The other flip-flop hold time violations are close to 0.

IV. CONCLUSION

This article presents a comparative study of several masterslaveflip-flops, taking into account process variability. Theirperformances are evaluated by looking at their timingcharacteristics like Clock-to-Q, Setup and Hold times. The approachcomprises of two phases. Pmf of codependent setup and hold time(CSHT) contours are determined by considering the probabilitydensity functions (pdf) of sources of variability in the first phase.A numerical backwards Euler based search is proposed tocharacterize CSHT efficiently and accurately.Simulations regarding these aspects and a functional study onreal paths allow to better classify their performances. It isclearly shown that the optimal FF is not the same for long andshort paths: a good setup time FF can have the worstperformances in hold time.

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